REMARKS

Claims 1 and 5 have been amended. No claims have been canceled or added. Claims 1-8 are pending.

Claims 1-3 and 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gowda (U.S. Patent No. 6,115,066). Claims 5-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Gowda in view of Adiletta (U.S. Patent No. 6,295,546). These rejections are respectfully traversed.

Claim 1 recites, *inter alia,* "each of said plurality of analog-to-digital converters comprising: a plurality of storage elements; and an analog-to-digital (ADC) portion, said ADC portion for receiving an analog signal from one of said pixel sensors of an associated logical unit when a selector element associated with said one pixel is enabled, and for converting said analog signal to a converted digital value, said ADC portion storing said converted value into one of said plurality of storage elements."

Claim 5 recites, *inter alia,* "receiving, in each of a plurality of A/D converter units each comprising a plurality of first storage unit, a plurality of second storage units, and an analog-to-digital conversion (ADC) portion, a respective plurality of signals from a respective plurality of first logical units, and A/D converting said respective plurality of signals into a respective plurality of converted digital values and storing said respective plurality of converted digital values information in a respective one of said plurality of first storage units."

Gowda is directed to a image sensor architecture. As shown in Fig. 3, Gowda discloses a image sensor architecture in which the pixels 30 of the image sensor are organized into columns $C_1 \ldots C_n$, wherein each column of pixels is associated with a respective column line $15_1 \ldots 15_n$. Associated with each column line $15_1 \ldots 15_n$ is an A/D

converter 40_1 ... 40_n. Each A/D converter 40_1 ... 40_n is coupled to a register 42_1 ... 42_n. Significantly, each one of the A/D converter 40_1 ... 40_n is coupled only a respective one of the plurality of register 42_1 ... 42_n. Gowda further discloses an alternative embodiment in which each A/D converter could be associated with plural column lines. However, even in this alternate embodiment, each A/D converter 40_i is still only associated with a single associated register 42_i. See column 4, lines 7-12 ("In the alternative, by incorporating a column select switch (not shown) on each column line 15_1-15_n, a smaller number of A/D converters 40 can be utilized, where each A/D converter would be tied to multiple column lines") and Fig. 3 (illustrating a one-to-one correspondence between A/D converters 40_i and registers 42_i).

Claims 1 and 5 have been amended to recite that each analog to digital converter includes an analog-to-digital (ADC) portion and a plurality of storage locations and that the analog to digital converter stores converted digital values in the plurality of storage locations. This feature is not taught or suggested by Gowda.

Claim 1 is therefore believed to be allowable over the prior art of record. Depending claims 2-4 are believed to be allowable for at least the same reasons as claim 1.

With respect to claims 5-8, the Office Action additionally cites to Adieletta. However, Adieletta does not cure the above noted deficiency with respect to the teachings of Gowda.

Claim 5 is therefore believed to be allowable over the prior art of record. Depending claims 6-8 are believed to be allowable for at least the same reasons as claim 5.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: August 26, 2004

Respectfully submitted,

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